**In the Claims**

This listing of claims will replace all prior versions, and listings, of claims.

**Listing of Claims**

1. (Previously presented) A method of fabricating a semiconductor memory device comprising:

providing a substrate;

sequentially forming a first conductive layer, a first type doped semiconductor layer, a first dielectric layer, a second type doped semiconductor layer on the substrate;

patterning the second type doped semiconductor layer, the first dielectric layer, the first type doped semiconductor layer, and the conductive layer along the first direction, thereby turning the conductive layer into a first conductive line;

etching the second type doped semiconductor layer, the first dielectric layer, and the first type doped semiconductor layer into a memory cell causing particulate silicon residues on the surface of the first conductive line;

depositing a second dielectric layer overlying the substrate, wherein oxygen plasma sputtering is employed to oxidize and remove the particulate silicon residues on the surface of the first conductive line before deposition;

planarizing the second dielectric layer to expose the memory cell; and

forming a second conductive line overlying the second dielectric layer, running generally orthogonal to the first conductive line.

2. (Original) The method according to claim 1, wherein the first type doped semiconductor layer is a $p^+$-type doped silicon layer.

3. (Original) The method according to claim 1, wherein the first conductive layer comprises a stack of TiN/$TiSi_2$/$p^+$-type doped silicon layers.

4. (Original) The method according to claim 1, wherein the first conductive line is a word line.

5. (Original) The method according to claim 1, wherein formation of the first dielectric layer comprises rapid thermal oxidation of silicon.

6. (Original) The method according to claim 1, wherein the second type doped silicon layer is n-type doped silicon layer.

7. (Original) The method according to claim 1, wherein the memory cell comprises a stack of $p^+$-type doped silicon/first dielectric/n-type doped silicon layers.

8. (Original) The method according to claim 1, wherein the step of oxygen plasma sputtering is performed using oxygen gas with a flow rate between about 300 and 400sccm.

9. (Original) The method according to claim 8, wherein the step of oxygen plasma sputtering is performed using argon gas at with a flow rate between about 200 and 250sccm.

10. (Original) The method according to claim 8, wherein the step of oxygen plasma sputtering is performed at a temperature within a range of about 225 to 275°C.

11. (Original) The method according to claim 7, wherein the step of oxygen plasma pre-sputtering is performed at a power within a range of about 1000 to 1500W.

12. (Original) The method according to claim 1, wherein the second conductive layer comprises a stack of $n^+$-type doped silicon/TiN/$TiSi_2$/$n^+$-type doped silicon/n-type doped silicon layers.

13. (Original) The method according to claim 1, wherein the second conductive line is a bit line.

14. (Previously presented) A method of fabricating one time programmable read only memory (OPTROM) device, comprising:

providing a substrate;

sequentially forming a stack of $p^+$-doped silicon layer/titanium silicide/titanium nitride/$p^+$-doped silicon layer/first dielectric/n-type doped silicon layers on the substrate;

patterning the stack of $p^+$-doped silicon layer/titanium silicide/titanium nitride/$p^+$-doped silicon layer/first dielectric/n-type doped silicon layers along the first direction, thereby turning the stack of $p^+$-doped silicon layer/titanium silicide/titanium nitride layers into a word line;

etching the stack of $p^+$-doped silicon layer/first dielectric/n-type doped silicon layers into a memory cell causing particulate silicon residues on the surface of the first conductive line;

depositing a second dielectric layer overlying the substrate, wherein oxygen plasma sputtering is employed to oxidize and remove the particulate silicon residues on the surface of the first conductive line before deposition;

planarizing the second dielectric layer to expose the memory cell; and

forming a stack of $n^+$-type doped silicon/ titanium nitride/ titanium silicide /$n^+$-type doped silicon/n-type doped silicon layers over the second dielectric layer and patterning the same into a bit line, running generally perpendicular to the word line.

15. (Original) The method according to claim 14, wherein formation of the first dielectric layer comprises rapid thermal oxidation of silicon oxide.

16. (Original) The method according to claim 14, wherein the step of oxygen plasma sputtering is performed using oxygen gas with a flow rate between about 300 and 400sccm.

17. (Original) The method according to claim 14, wherein the step of oxygen plasma sputtering is performed using argon gas with a flow rate between about 200 and 250sccm.

18. (Original) The method according to claim 14, wherein the step of oxygen plasma sputtering is performed at a temperature within a range of about 225 to 275°C.

19. (Original) The method according to claim 14, wherein the step of oxygen plasma pre-sputtering is performed at a power within a range of about 1000 to 1500W.

20-25. (Cancelled)

26. (Previously presented) A semiconductor memory device fabricated by the process as claimed in claim 1.

27. (Previously presented) A semiconductor memory device fabricated by the process as claimed in claim 14.